

## **REMARKS**

Claims 1-12 are pending in the application. It is gratefully acknowledged that Claims 6 and 8 have been objected to by the Examiner as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims. Claim 10 was objected to because of informalities. Claims 1-5, 7 and 9-12 were rejected under 35 U.S.C. §102(e) as being anticipated by Suda et al. (U.S. Patent 6,553,516).

In the previously filed Response, the element “inter-row permutation pattern T(j)” was mistakenly changed to “intra-row”. Claim 10 is shown above correcting this mistake. Withdrawal of the objection of Claim 10 is respectfully requested.

Regarding independent Claim 1, the Examiner states that Suda et al. anticipates all of the elements of this claim. Suda et al. discloses an interleaving method, interleaving apparatus, turbo encoding method, and turbo encoder. First, the Examiner states that an address table used during the second stage intra-permutation (col. 5, lines 53-55) anticipates the register for updating and registering a plurality of parameters for setting an operating condition of the interleaver recited in Claim 1. However, an address table by definition does not update and register a plurality of parameters, but merely stores addresses. Second, Claim 1 recites an address calculator (an element which the Examiner does not make reference to) for generating a finally interleaved address; the finally interleaved address is generated by using an inter-row permutation pattern T(j), an intra-row permutation pattern increment arrangement value incr(j) and an intra-row permutation basic sequence s(i) provided from the register. The closest thing to an address calculator in Suda et al. is the address table, and by definition, a table is not a calculator. The Examiner cites an inter-permutation and computing an intra-row permutation mapping sequence c(i) to allegedly anticipate these elements. The intra-row permutation sequence of Suda et al. is not the intra-row permutation pattern increment arrangement value recited in Claim 1. Suda et al. does not teach or disclose the intra-row permutation pattern increment arrangement value recited in Claim 1. Since every element of Claim 1 is not taught by Suda et al., the reference cannot

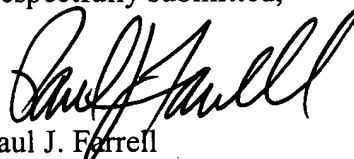
anticipate the claim. Based on at least the foregoing withdrawal of the rejection of Claim 1 is respectfully requested.

Regarding Claim 10, the Examiner states that Suda et al. discloses all of the elements of this claim. Although Suda et al. might disclose an inter-row permutation, Suda et al. does not calculate an increment value  $\text{incr}(j)$  for generating an intra-row permutation pattern  $a(j)$  using the permuted inter-row address as recited in Claim 10. Further Suda et al does not disclose calculating an intra-row permutation pattern using the increment  $\text{incr}(j)$  and a previous intra-row permutation pattern. Since every element of Claim 10 is not taught by Suda et al., the reference cannot anticipate the claim. Based on at least the foregoing withdrawal of the rejection of Claim 10 is respectfully requested.

Independent Claims 1 and 10 are believed to be in condition for allowance. Without conceding the patentability per se of dependent Claims 2-5, 7, 9, 11 and 12, these are likewise believed to be allowable by virtue of their dependence on their respective amended independent claims. Accordingly, reconsideration and withdrawal of the rejections of dependent Claims 2-5, 7, 9, 11 and 12 is respectfully requested.

Accordingly, all of the claims pending in the Application, namely, Claims 1-12, are believed to be in condition for allowance. Should the Examiner believe that a telephone conference or personal interview would facilitate resolution of any remaining matters, the Examiner may contact Applicant's attorney at the number given below.

Respectfully submitted,



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